The Investigation of Source Field Plate on the Performance of pGaN Gate Device and Dual-Gate Bidirectional Switch using TCAD Simulation

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***Abstract*—This paper presents the investigation of the source field plate geometry on the p-GaN/GaN/AlGaN HEMT bidirectional switch using TCAD simulation. The output and transfer characteristics of both single-gate and dual-gate GaN devices are obtained. Moreover, the impact of the source field plate on the dynamic on-resistance of the p-GaN gate device is verified. Building upon previous research on field plates, this study examines the field plate's influence on breakdown voltage from two perspectives. The first aspect considers the number of field plate layers. Adjusting the length of the two field plate layers shows that the breakdown voltage could reach a peak value. The second aspect focuses on the field plate geometry. Increasing the transverse and longitudinal distance between the field plate and the gate effectively enhances the device's breakdown performance.**

Keywords—Gallium Nitride, Bidirectional Switch, Field Plate, Dynamic On-resistance, Breakdown Voltage

I. INTRODUCTION

Gallium Nitride (GaN) is a promising wide band-gap semiconductor material with significant advantages in device performance and efficiency [1] [2]. The GaN device's notable feature is the ability to operate at higher voltages due to its high critical electric field, it also exhibits lower on-resistance and higher switching speed. The utilization of GaN High Electron Mobility Transistor (HEMT) devices in power electronics has garnered considerable attention. Researchers have explored various field plate configurations to enhance breakdown voltage, dynamic performance, and reliability by modifying the electric fields between the gate and drain region [3]. This improvement is achieved by redistributing the quantity and position of the electric field peaks using gate and source field plates [4–6]. The researchers examined the relationship between the field plate structure and electric field distribution by modeling the devices and systematically adjusting structural parameters. The changes in breakdown voltage were analyzed based on the variations in electric field distribution.

Despite the advantages of GaN-based power HEMTs, they still face challenges related to traps and other degradation mechanisms that can negatively impact their dynamic performance and reliability. In particular, dynamic on-resistance degradation caused by charge trapping in buffer stacks or on surfaces has emerged as a significant obstacle for GaN-based devices [7-9]. Addressing this issue is crucial for further enhancing the performance and reliability of GaN-based power HEMTs. Different field plate structures have improved dynamic on-resistance performance [10]-[12]. Furthermore, the bidirectional switch is a device that has bidirectional conduction and blocking capabilities at specific states. The device has a novel dual-gate structure to realize the bidirectional operation in AC-related power conversion applications. The common drain area between two gates can also be adjusted to reduce the peak electric field, ultimately increasing the breakdown voltage [13].

In this work, we first discuss the static characteristics of the bidirectional switch. Subsequently, we confirm the effect of the field plate on the on-resistance through TCAD simulations, demonstrating the improvement in the device's dynamic characteristics. Building upon this analysis, we investigate the influence of the source field plate on the device's breakdown from two dimensions: the number of field plates and their geometries. These discussions provide valuable insights into the design of bidirectional switches.

II. DEVICE MODELING

A. Device Structure

Figure 1 illustrates the cross-section view of the dual-gate pGaN/AlGaN/GaN bidirectional switch. The device is based on a 2000 nm AlGaN buffer layer. To form a two-dimensional electron gas (2DEG), a 10 nm GaN channel layer and a 15 nm AlGaN barrier layer are added on top of the buffer layer. The pGaN layers beneath both gate areas have a consistent thickness of 110 nm. Additionally, a passivation layer with a thickness of 390 nm is applied to the top. Table I provides the parameters used to obtain the general I-V characteristics of the dual-gate device. The thickness and length of each layer can vary depending on the investigation.

As the device has a symmetric structure, the S1 and S2 terminals can be interchanged based on the connection method. When S1 is connected to the voltage supply, and S2 is connected to the ground, the S1 terminal functions as the drain, and S2 acts as the source, and vice versa.

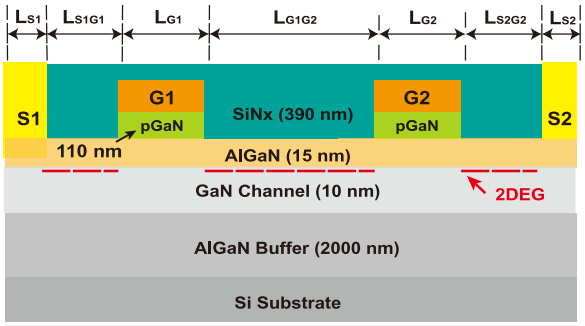

Fig. 1 Cross-section view of the dual-gate pGaN/AlGaN/GaN HEMT.

TABLE I
DEVICE PARAMETERS

Symbol	Quantity	Values
L_{S1}	S1 terminal length	0.5 µm
L_{S2}	S2 terminal length	0.5 µm
L_{S1G1}	S1 to G1 separation	1 µm
L_{S2G2}	S2 to G2 separation	1 µm
L_{G1}	G1 terminal length	1.4 µm
L_{G2}	G2 terminal length	1.4 µm
L_{G1G2}	G1 to G2 separation	3.6 µm
$t_{barrier}$	thickness of AlGaN barrrier	15 nm
$t_{channel}$	thickness of GaN channel	10 nm
t_{buffer}	thickness of AlGaN Buffer	2 µm
$t_{passivation}$	thickness of passivation layer	390 nm
$x_{barrier}$	mole fraction of Al in barrier	23%
x_{buffer}	mole fraction of Al in buffer	5%
$N_{p\text{-}GaN}$	actived B doping concentration of p-GaN layer	3×10^{17} cm^{-3}
$N_{Barrier}$	concentration of AlGaN barrier	1×10^{15} cm^{-3}
$N_{Channel}$	concentration of GaN channel	1×10^{15} cm^{-3}
N_{Buffer}	concentration of AlGaN buffer	1×10^{15} cm^{-3}

B. *Modeling Procedure*

The device structure editor (SDE) is utilized to model the dual-gate GaN HEMT. This study employs single-layer and two-layer field plates to examine the impact of field plate-related factors on the device's breakdown voltage. An avalanche model is used for the breakdown simulation to accurately represent the device's characteristics. The traps in the buffer layer are acceptor traps, with a concentration of 1×1015 cm-3 and an energy level of 0.45 eV relative to the bottom of the conduction band. Moreover, the passivation and AlGaN interface traps are donor traps, with a concentration of 5×1019 cm-3 and an energy level of 0.6 eV relative to the mid-bandgap. Tunneling models are applied to the S1 and S2 terminals to simulate ohmic contacts, while the Shockley-Read-Hall (SRH) model is employed to simulate the electron-hole recombination process. Additionally, polarization models account for the polarization effect at the GaN/AlGaN interface, contributing to the formation of the 2DEG.

III. RESULTS AND DISCUSSIONS

A. *General I-V Characteristics*

Figure 2 (a) compares the output characteristic curves for single and dual gate devices, where G1 and G2 are connected, ranging from -7 V to 7 V with a step size of 1 V. Figure 2(b) displays their transfer characteristics. Notably, the threshold voltage for both devices remains consistent at 0.9 V. Both devices exhibit favorable forward and reverse conduction characteristics. As shown in Figure 3, to verify the diode mode conduction for the bidirectional switch, the device operates in diode mode when the gate terminal G2 is connected to S2 and G1 is connected to the applied voltage. Under DC conditions, as the voltage in S2 increases, the output drain current (I_{S2S1}) does not immediately rise but increases once the applied S2 voltage surpasses the device's threshold voltage. Conversely, the device transitions to the cut-off state if the drain voltage is applied to S1 while the terminals G2 and S2 are connected to the ground. In this scenario, no reverse conduction current is observed. Under AC conditions, a sinusoidal signal with a frequency of 100 kHz is only displayed on the positive axis, while the signal on the negative axis is completely blocked.

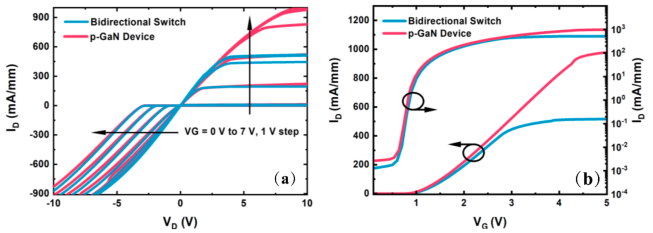

Fig. 2 The (a) Output and (b) Transfer characteristics of the single-gate and dual-gate GaN device.

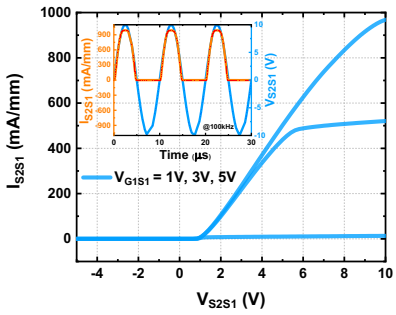

Fig. 3 Output characteristic of dual-gate GaN device in diode mode under DC power supply. (Inset: Output characteristic of dual-gate GaN device in diode mode under AC power supply)

B. *Field Plate Structure for Dynamic R_{on} Performance*

This section investigates the impact of a single-layer source field plate (FP) on a single-gate device, aiming to elucidate how field plates contribute to improving dynamic Ron performance. Figure 4 illustrates the cross-section of the device structure. The simulation procedure employed in this study is outlined as follows. Initially, a high drain voltage is applied for 10 ms at the off state, followed by the measurement time through a 5 V signal for 10 ms at the on state. As depicted in Figure 6, analysis of the obtained results reveals a clear trend: the dynamic on-resistance (Dynamic Ron) to static on-resistance (Static Ron) ratio increases as the stress voltage is raised. Notably, a significant finding of this investigation is that an increase in the number of field plates reduces the dynamic Ron, effectively mitigating the occurrence of current collapse phenomena.

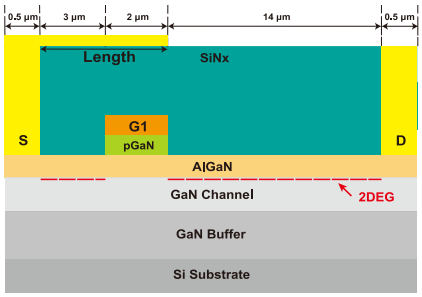

Fig. 4 Schematic diagram of the device for testing dynamic R_{on}.

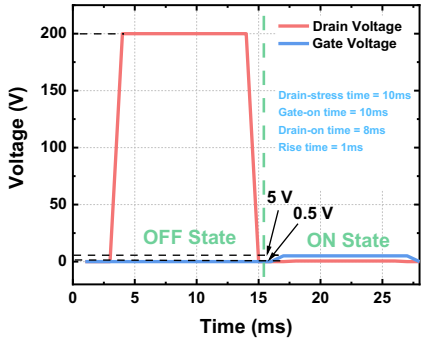

Fig. 5 Demonstration of the transient simulation setup. (Drain-stress time = 10 ms, Measurement time = 10 ms)

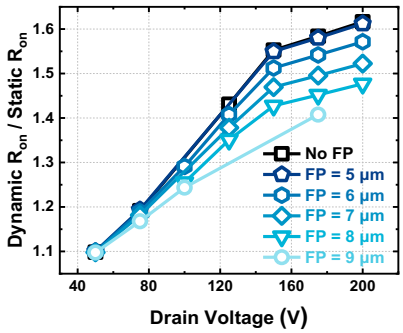

Fig. 6 Results of dynamic R_{on} under different lengths of field plate.

C. *Two-layer Source Field Plate on Dual-gate Device*

This section employs the two-layer field plate structure to investigate the breakdown voltage performance. The thickness of the passivation layer is extended to 800 nm. The upper field plate is positioned on top of the passivation layer, while the lower field plate is positioned 320 nm away from the upper field plate and 200 nm above the gate terminal. Analysis of the 3D plot in Figure 8 reveals that the breakdown voltage does not increase with the extension of the field plate length. However, once the field plate length reaches a certain threshold (specifically, when the lower field plate is 2.7 μm and the upper field plate is 3.6 μm), the breakdown voltage reaches a peak value of approximately 1478 V, after which it starts to decline.

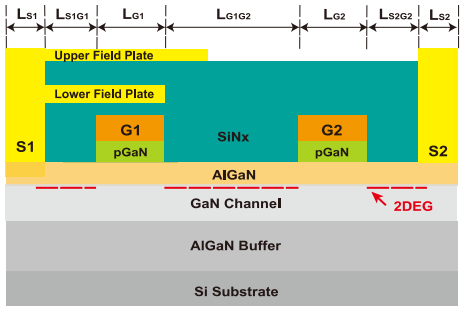

Fig. 7 Cross-section view of the two-layer field plate of the dual-gate bidirectional switch.

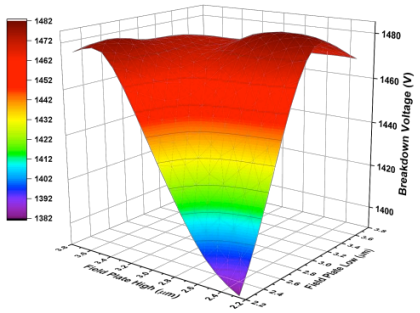

Fig. 8 3D view of the relationship of the breakdown voltage against the upper field plate and lower field plate.

D. *Source Field Plate Geometry on Dual-Gate Device*

Unlike the previous section, field plates are added to both device terminals in this section to investigate the correlation of field plates between the two sides. However, the original device length must be increased to accommodate field plates on both sides, necessitating an extension of the device length. Based on the findings from section C, it is observed that the impact of the two layers of field plates on the breakdown voltage is nearly identical. As a result, in this particular section, the field plate is simplified to a single-layer configuration, and the geometry of the field plate on the breakdown voltage of the bidirectional switch is investigated. S1 to G1 and S2 to G2 are separated to 3 μm. The G1 and G2 terminal lengths are changed to 5 μm while G1 to G2 separation is changed to 9 μm. The definition of three structural parameters corresponding to different dimensions is marked in the figure: Xll is the horizontal distance between FP and Gate, and Yll is the vertical distance between FP and Gate. Length is the Effective length of FP. By observing results, it can be easily found that breakdown voltage increase with increment of Xll and Yll separately; however, there is almost no BV change while changing the length of FP. This is because the length of the two-gate device is a little short. The distance between the two source field plates is too small, which means that the distance between the source and drain is shortened, and high voltage can be brought from the drain to the source through the source FP in the drain, reducing the stability of the device.

IV. CONCLUSION

The study investigates the impact of field plate geometry on the performance of p-GaN gate devices and dual-gate bidirectional switches using TCAD simulation. The paper first discusses the general static characteristics of the dual-gate

device to validate its design rationale. Subsequently, this paper demonstrates that the field plate effectively reduces the dynamic on-resistance of the p-GaN single-gate device. Building upon these findings, we explore the application of a single-sided, double-layer field plate to the bidirectional switch, observing that the breakdown performance can be significantly enhanced by increasing the length of the field plate. Recognizing the symmetry characteristics of the bidirectional switch, the final section applies the field plate to both the S1 terminal and S2 terminal of the device. Remarkably, it is discovered that increasing the distance between the field plate and the gate leads to an amplified breakdown voltage in the bidirectional switch, offering valuable insights for the future design of bidirectional switches with high operating voltage.

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